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09/963,924	09/26/2001	Yoshikazu Kasuya	15.49/6067	1276

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EXAMINER
RAO, SHRINIVAS H

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/21/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/963,924	Applicant(s) KASUYA, YOSHIKAZU
	Examiner Steven H. Rao	Art Unit 2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 November 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 September 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

Priority

Receipt is acknowledged of paper submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file claiming priority from Japanese Patent Application No. 2000-292143(P) filed on September 26, 2000.

Election/Restrictions

Applicant's election without traverse of claims 1-17 and 20-21 in Paper No. 7 is acknowledged.

Drawings

The drawings filed on September 26, 2001 have been accepted by the draftsperson.

Specification

The disclosure is objected to because of the following informalities: specification page 1 lines 5-12 applicants' refer to two co-pending U.S. applications that are related to this case by attorney docket numbers only, however as applications now have the serial numbers of these applications, they (the related applications) must be identified by their serial numbers also.

Appropriate correction is required.

Preliminary Amendment

Applicants' amendment faxed on November 13, 2002 ahs been entered on November 13, 2002.

Therefore claims 18-21as originally filed are cancelled and claims 1-17 as originally filed are currently pending in the application.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-17are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claims 1, 7 and 13 the phrase "conduction layer renders the claim indefinite because the term "conduction layer " is indefinite. If applicants' mean " conductive layer". It is suggested that all occurrences of " conduction layer " be replaced with " conductive layer ".

Claims 2-6, 8-12 and 14-17 are rejected for at least depending directly or indirectly upon rejected claims 1, 7and 13.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Misra et al. (U. S. Patent No. 5,960,270 herein after Misra, also cited by applicants' in their Ids).

With respect to claim 1, Misra describes a method of manufacturing a semiconductor device including the steps of : forming a gate dielectric layer (fig. 10 # 105), forming a first conductive layer having a specified pattern on the gate dielectric layer (Fig. 11 # 108), forming a first upper layer comprising a material different from the first conductive layer on the first conductive layer (fig. 111 # 110), forming a second upper layer comprising a material different from the first upper layer on the first upper layer (fig. 14 # 120) forming sidewall spacers on side walls of the first conductive layer, the first upper layer and the second upper layer (Fig. 14 # 114), forming an insulating layer that covers the second upper layer and the side wall spacers (Fig. 14 # 122), planarizing the insulation layer until an upper surface of the first conduction layer is exposed (fig. 15, planarize 122) , remove the second upper layer (fig. 15) removing the first upper layer to from a recessed section between the sidewall spacers (fig. 16), forming a second conductive layer in the recessed section to from a gate electrode that includes at least the first conductive layer and the second conductive layer (fig. 17 # 128) It is noted that the figs. 19-22 show a second embodiment, however as stated in col. 10 lines 37-39, the steps describing the embodiment in figs. 10-16 are also used in the embodiment described in figs. 19-22 filling a second conduction layer in the recessed section to form a gate electrode that includes at least the first conduction layer and the second conduction layer.

It is noted that Misra does not describe the forming the upper layers and the sidewall spacers in the same sequence as recited in the claims, however it is noted that applicants' use the term " comprising" which does not exclude other sequences and further it is well settled that , " As a matter of fact selection of any order of performing process steps is prima facie obvious in the absence of new or unexpected results." In re Burhaus, 154 F.2d 690, 69 USPQ 330 (CCPA 1946) and also Ex parte Rubin, 1126 USPQ 440 (BAPI 1959).

Therefore the teachings of Misra are prima facie obvious even if the steps are performed in different sequence without a showing of new or unexpected results.

With respect to claim 2, wherein step (h) is conducted by an etching method (Misra col. 9 lines 60-67) and in the step (h), a ratio of an etching rate of the second upper layer with respect to an etching rate of the first upper layer is two or greater. (It is an inherent property that the etching rate of Misra's polysilicon layer 128 with respect to Misra's nitride layer 120 is two or greater as the etching rate of a particular material for a particular etchant is an inherent property of that material and as the same materials are used in the Misra reference as that used by applicants' in their specification page e.g. 11-12 and what ever inherent properties is inherent to the materials used by applicants is also true (inherent) for the same materials in the same situation for the Misra reference also).

With respect to claim 3, wherein the step (i) is conducted by an etching method , and in step (i) a ratio of an etching rate of the first upper layer with respect to an etching rate of the first conductive layer is two or greater . (It is an inherent property that the

etching rate of Misra's nitride layer 120 with respect to the Misra's conductive polysilicon layer 108/128 is two or greater and similar to the description by applicants' in their specification page e.g. 11-12 and further the same arguments as stated under claim 2 above are incorporated here by reference).

With respect to claim 4, wherein the first upper layer is formed from silicon nitride (Misra layer 120 from silicon nitride) and the second upper layer is formed from polysilicon. (Misra layer 108/128).

With respect to claim 5, wherein after step (i) forming a barrier layer between the first conduction layer and the second conduction layer . (Misra fig. 20, col. 10 lines 39-30, not shown in fig. 20).

With respect to claim 6, after step (i) forming a barrier layer between the first conductive layer and the second conduction layer and forming a barrier layer between the second conduction layer and the sidewall spacers (Fig. 2 C # 60 and Fig. 2D).

With respect to claim 7, Misra describes the method for manufacturing a semiconductor device includes the steps of : forming a gate dielectric layer(Misra fig.10 # 105), forming a first conductive layer on the gate dielectric layer (Misra Fig. 1 F # 28, col. 6 lines 41-42), forming an upper layer on the first conductive layer, at least a lower portion of the upper layer comprising a material different from at least an upper portion of the first conductive layer (fig. 2b # 32, col. 8 lines 8-10 fig. 2b # 32, col. 8 lines 8-10), forming sidewall spacers on side walls of the first conductive layer and the upper layer (Misra fig. 5), forming an insulation layer that covers the upper layer and the sidewall spacers (fig. 7 # 30), planarizing the insulation layer until an upper surface of the upper

layer is exposed (fig. 8), removing the upper layer to form a recessed section between the sidewall spacers on an upper portion of the first conductive layer (fig. 9) and forming the second conductive layer in the recessed section to form a gate electrode that includes at least the first conductive layer and the second conductive layer(fig. 9 # 36).

With respect to claim 8, wherein after step (g) is conducted by an etching method and in step (g), ratio of an etching rate of at least the lower portion of the upper layer with respect to an etching rate of the at least upper portion of the first conductive layer is two or greater . (rejected for reasons stated under claim 2 above) .

With respect to claim 9, wherein the first conduction layer is formed from a poly silicon layer (Misra col.9 line 64).

forming a barrier layer between the first conduction layer and the second conduction layer (Fig. 2 A # 54, col. 7 line 39, col. 8 lines 53-59).

With respect to claim 10, wherein the second conduction layer comprises a material selected from the group consisting of a metal, a metal alloy and a metal compound (Misra layer 128).

With respect to claim 11, wherein after step (g) forming a barrier layer between the first conductive layer and the second conductive layer (rejected for same reasons as stated under claim 5 above).

With respect to claim 12, wherein after step (g) forming a barrier layer between the first conductive layer and the second conductive layer and forming a barrier layer between the second conductive layer and the sidewall spacers (Misra col.9 lines 55-60).

With respect to claim 13, wherein the method of manufacturing a semiconductor device includes the steps of : forming a gate dielectric layer (fig. 10 # 105), forming a first conductive layer on the gate dielectric layer (fig.11 # 108), forming an upper layer on the conductive layer (fig. 12 # 114), forming sidewall spacers on side walls of the first conductive layer and the upper layer (fig. 14 # 120), removing the upper layer to form a recessed section between the sidewall spacers and above at least part of the conductive layer (fig. 16), and forming a second conductive layer in the recessed section to form a gate electrode comprising the at least part of the first conduction layer and the second conduction layer .(fig. 21).

With respect to claim 14, wherein after step (g) forming a barrier layer between the first conductive layer and the second conductive layer (rejected for the same reasons as stated under claim 5 above).

With respect to claim 15, wherein after step (g) forming a barrier layer between the first conductive layer and the second conductive layer and forming a barrier layer between the second conductive layer and the sidewall spacers (rejected for the same reasons as stated under claim 6 above).

With respect to claim 16, wherein the first conductive layer and the second conductive layer comprises materials having different compositions. (rejected for same reasons as stated under claim 4 above).

With respect to claim 17, wherein the first conductive layer comprises polysilicon and the second conductive layer comprises a material selected from the group

consisting of a metal, a metal alloy and a metal compound. (Misra fig. 12 # 108 – polysilicon and fig. 19 # 129- metal).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven H. Rao whose telephone number is (703) 3065945. The examiner can normally be reached on 8.00 to 5.00.

The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-3926 for regular communications and (703) 872-9319 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 306-7722.

Steven H. Rao

Patent Examiner

November 15, 2002

SUPERVISORY PRIMARY EXAMINER
TECHNOLOGY CENTER 2800